REMARKS

Claim Objections

The claims 1 and 7 are objected to because of informalities.

Claim1 is amended, as needed, to overcome this objection. Claim 7 is deleted without prejudice thus rendering any rejection applied thereto moot. Reconsideration and withdrawal of this objection are respectfully requested.

Claim Rejections under 35 U.S.C. §112

Claims 1, 2, 4-6 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards the invention.

Relevant claims have been amended, as needed, to overcome this rejection. Reconsideration and withdrawal of this objection are respectfully requested.

Claim Rejections under 35 U.S.C. §102

Claims 1, 4, 6 and 7 are rejected under 35 U.S.C. 102(e) as being anticipated by Lin et al. (USP 6,359,340).

Upon review of independent claim 1, it is learned that there were typographical mistakes regarding the first and second plurality of pads. Upon correction of this mistake, claim 1 is patentably distinguished over the asserted prior art.

In view of the difficulty the Office had regarding what the "side surface" referred to, relevant

portion of claim 1 has been amended. Specifically, a side substrate side surface is introduced to substrate 12 and a plate member side surface is introduced to plate member 20. As shown by way of an example in Figure 2, indeed there is shown a plate member side surface 20a and a substrate side surface that is unlabeled however is sharing a same imaginary plane as the plate member side surface 20a.

In contradistinction, in Figure 10 of Lin et al., there are no side surfaces of the substrate 560 sharing an imaginary plane with any side surface of plate member 520.

Independent claims 1, as amended, is fully supported by way of an example in Figures 1-2 and associated written description. Looking at Figures 1-2, there is indeed shown a semiconductor device comprising a substrate 12 having a substrate side surface (adjacent to labels 20a, 36a, 20, 26), a first plurality of pads 14 and a second plurality of pads 15; a first semiconductor chip 18 mounted on said substrate 12 and having a third plurality of pads 24; a plate member 20 arranged on said first semiconductor chip 18 having a first end at an inward position of said first semiconductor chip 18 adjacent to the third plurality of pads 24, and a second end having a plate member side surface 20a sharing a same imaginary plane with said substrate side surface 36a; a second semiconductor chip 22 arranged on said plate member 20 having a fourth plurality of pads 26; a first structure 32 and a second structure 34 respectively and electrically inter-connecting said third plurality of pads 24 of said first semiconductor chip 18 with said second plurality of pads 15 of said substrate 12 and said fourth plurality of pads 26 of said second semiconductor chip with said first plurality of pads of said substrate 14; and the seal member 36 sealing said first semiconductor chip 18 and said second semiconductor chip 22.

It is well settled that:

"A claim is anticipated only if each and every element *as set forth in the claim* is found, either expressly or inherently described, in a single prior art reference." *Constant v. Advanced Micro-Devices, Inc.*, 848 F.2d 1567, 7 USPQ2d 1057 (Fed. Cir. 1988)."

The Office Action has mentioned on page 4 of the Office Action that "a package" is inherently describing packaging/encapsulating/sealing of the device. In the package, the chip is wholly embedded in the sealing resin for the protection of the chip. If the chip is exposed to the outside of the sealing resin, the protection function is lost. Therefore, the chip is not exposed to the outside of the sealing resin. Other members are also not exposed to the outside of the sealing resin.

Should the Office continue to assert that the claimed invention, as amended, is anticipated by the asserted prior art, a citation of where each and every claimed feature, either as column number and line number, or figure number and reference numeral, or a combination thereof, as disclosed in the asserted prior art is respectfully requested.

Should the Office determine that any claimed feature is not disclosed in the asserted prior art, it is respectfully submitted that the claimed invention is thereby not anticipated by the asserted prior art. Allowance of the claimed invention is then respectfully requested.

CONCLUSION

It is respectfully submitted that the claimed invention, as amended, patentably distinguishes over the asserted prior art. Claims dependent thereon, by virtue of inherency, also patentably distinguish over the asserted prior art. Reconsideration and withdrawal of this rejection are respectfully requested.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "**Version with markings to show changes made**."

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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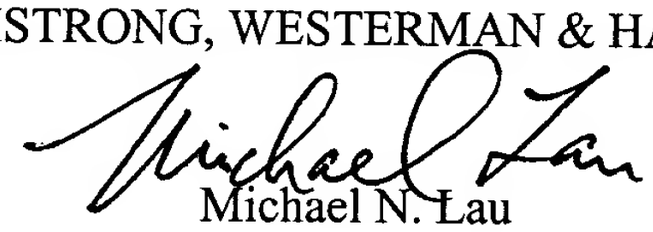

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PATENT TRADEMARK OFFICE

Enclosures: Version with markings to show changes made
Request for Approval of Drawing Corrections w/Figs1-4 marked in red ink
Substitute Abstract of the Disclosure

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VERSION WITH MARKINGS TO SHOW CHANGES MADE 09/973,002

IN THE CLAIMS:

Proposed Claim Amendment:

1. (Twice Amended) A semiconductor device comprising:

a substrate having a first plurality of pads and a second plurality of pads;

a first semiconductor chip mounted on said substrate and having a third plurality of pads;

a plate member arranged on said first semiconductor chip and having an [a first] end at an inward position of said first semiconductor chip adjacent [from] to the third plurality of pads[, and a second end being exposed to an outside of a seal member through a side surface thereof];

a second semiconductor chip arranged on said plate member and having a fourth plurality of pads;

a first structure and a second structure respectively and electrically interconnecting said third plurality of pads [of said first semiconductor chip] with said first plurality of pads [of said substrate] and said fourth plurality of pads [of said second semiconductor chip] with said second plurality of pads [of said substrate]; and

a [the] seal member sealing said first semiconductor chip, said plate member and said second semiconductor chip[.] and having a seal member side surface;

wherein said plate member has a first portion covered by said first and second semiconductor chips, and a second portion protruding from said first and second semiconductor chips and extending through said seal member to the seal member side surface whereby said plate

member is exposed to an outside of said seal member.

2. (Amended) A semiconductor device according to claim 1, wherein said first structure and said second structure [electrically connecting said third plurality of pads of said first semiconductor chip and said fourth plurality of pads of said second semiconductor chip respectively to said first plurality of pads of said first semiconductor chip and said fourth plurality of pads of said second semiconductor chip respectively to said first plurality of pads and said second plurality of pads of said substrate by] are made of bonding wires.

5. (Twice Amended) A semiconductor device according to claim 1, wherein said plate member includes a fifth plurality of pads [and a sixth plurality of pads, a third structure and a fourth], part of said second structure [respectively and] electrically inter-connecting [said third plurality of pads of said first semiconductor chip with said first plurality of pads of said substrate and] part of said fourth plurality of pads [of said second semiconductor chip] with part of said second [first] plurality of pads [of said substrate] via said fifth plurality of pads. [;

wherein a first member electrically connecting said fourth plurality of pads of said second semiconductor chip with said sixth plurality of pads of said plate member and a second member electrically connecting said fifth plurality of pads plate member with said second plurality of pads.]